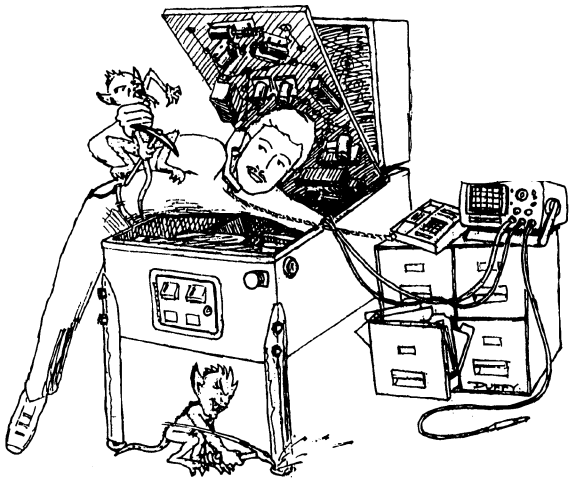
Service Bulletin Nº 75

SEGA™
PINBALL, INC.
1990 Janice Avenue
Melrose Park, IL 60160
• ✆ Tel 708-345-7700 •

Technical Support

• 1-800-KICKERS (800-542-5377) •
• Fax 708-345-7889 •



Joe Blackwell	Eric Winston	Ted Kilpin	Jay Alfer
Technical Support Manager	Technical Support Engineer	Technical Support Engineer	Tech. Doc. Administrator

TO: Parts & Service Managers

DATE: June 1, 1995

RE: **CPU Board - *Blanking* Circuit Theory Of Operation**

We think it is time to answer some of the questions we have been asked from time to time regarding the diagnostic L.E.D.'s on the CPU board (e.g. What should my ***blanking*** be doing? Your ***blanking*** is doing what? or What the ***blanking*** are you talking about?).

The ***blanking circuit*** on the CPU operates on a concept similar to that of the "watchdog reset" which has been used for years in our industry. As long as the program for the game is running correctly, the output of the ***blanking circuit*** (which is a 555 timer configured as a missing pulse detector (see Fig. 1 & 2) is in it's "normal" state - in our case a logic "1" or "hi". If for some reason the board stops running the game program, the ***blanking circuit output*** drops to a logic "0" or "low". This is a fault condition, and this "low" signal is gated to all solenoid drivers as well as lamp matrix column drives so that these outputs are disabled if a board fault triggers the ***blanking circuit***.

The missing pulse detector action of the ***blanking*** circuit is controlled by the T.G. signal developed at the PA2 (pin 4) output of PIA 11B (see Fig. 3). In the old days of segmented displays this was one of four address signals that were decoded to digit select strobes. This line is toggling at a known rate with a period of 2.8 mS. These address signals are generated by the game program; so if the program stops running, these address signals stop toggling, and the electronics in the Missing Pulse Detector ***circuit*** (starting at pin 9 of IC 6F (7404 inverter) through to pin 3 of IC 1C (555 timer) (the ***blanking circuit output***) generate the "fault" state with the ***blanking output*** low or "0".

The ***blanking circuit*** is self-resetting; if the program is restarted after a fault or "hang-up" the ***blanking circuit output*** returns to the "normal" state of "hi" or "1". Another function of the ***blanking circuit*** is to hold the outputs that it controls in a disabled state for a short period of time at board power-up. This ensures that these outputs are not active during the time that the CPU is performing power up initialization.

"May the ***blanking*** be With You."

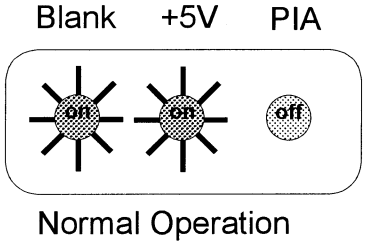
Special Note:

Power-Up CPU Self Tests

Upon power-up, the **CPU** Board performs a series of self tests of major components. Turn the game on while observing the **LEDs** on the **CPU** Board. Tests of the **PIAs**, **RAM**, and **EPROMs** are performed automatically and results of the tests are indicated by the **PIA LED**.

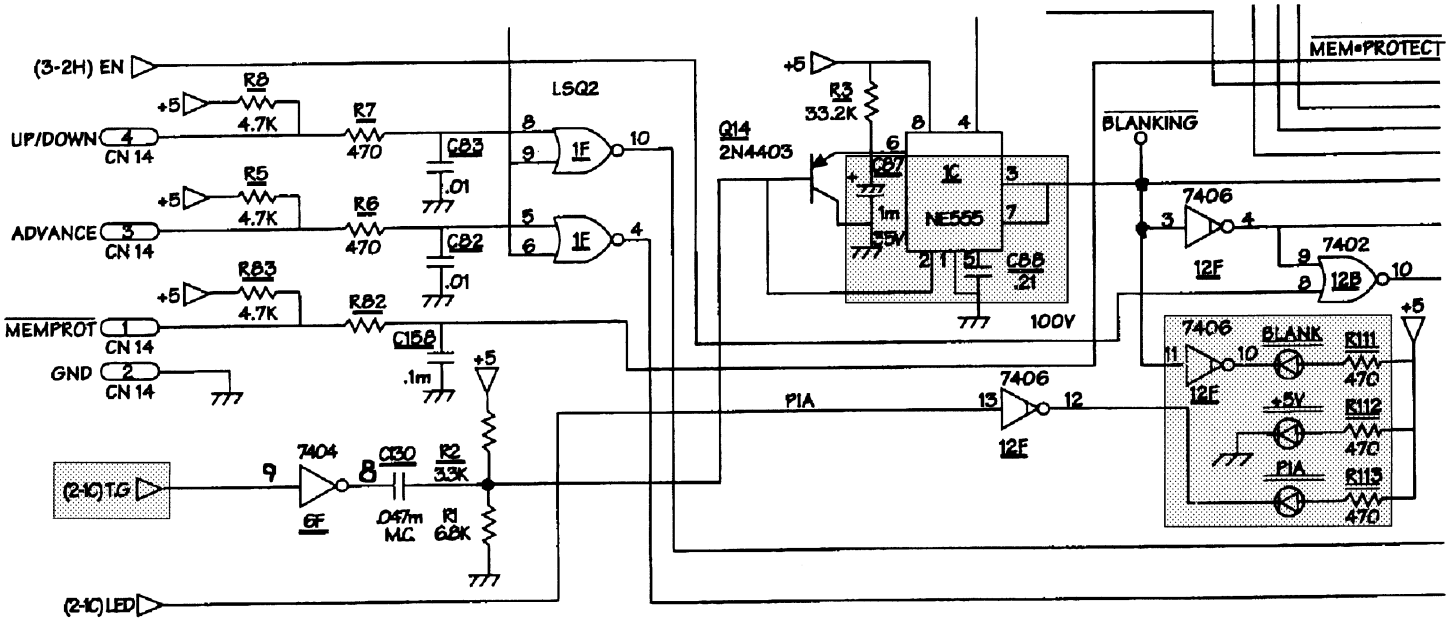
With all tests passed, the **LEDs** illuminate in the following sequence at power turn-on. The **PIA** and +5v **LEDs** illuminate immediately. Approximately ½-second later, the **PIA LED** goes out and the ***blanking*** **LED** illuminates; the ***blanking*** and +5v **LEDs** remain illuminated (normal operation) until the game is turned off (see Fig. 1). Test failures are indicated with the **PIA LED** lit.

Fig. 1



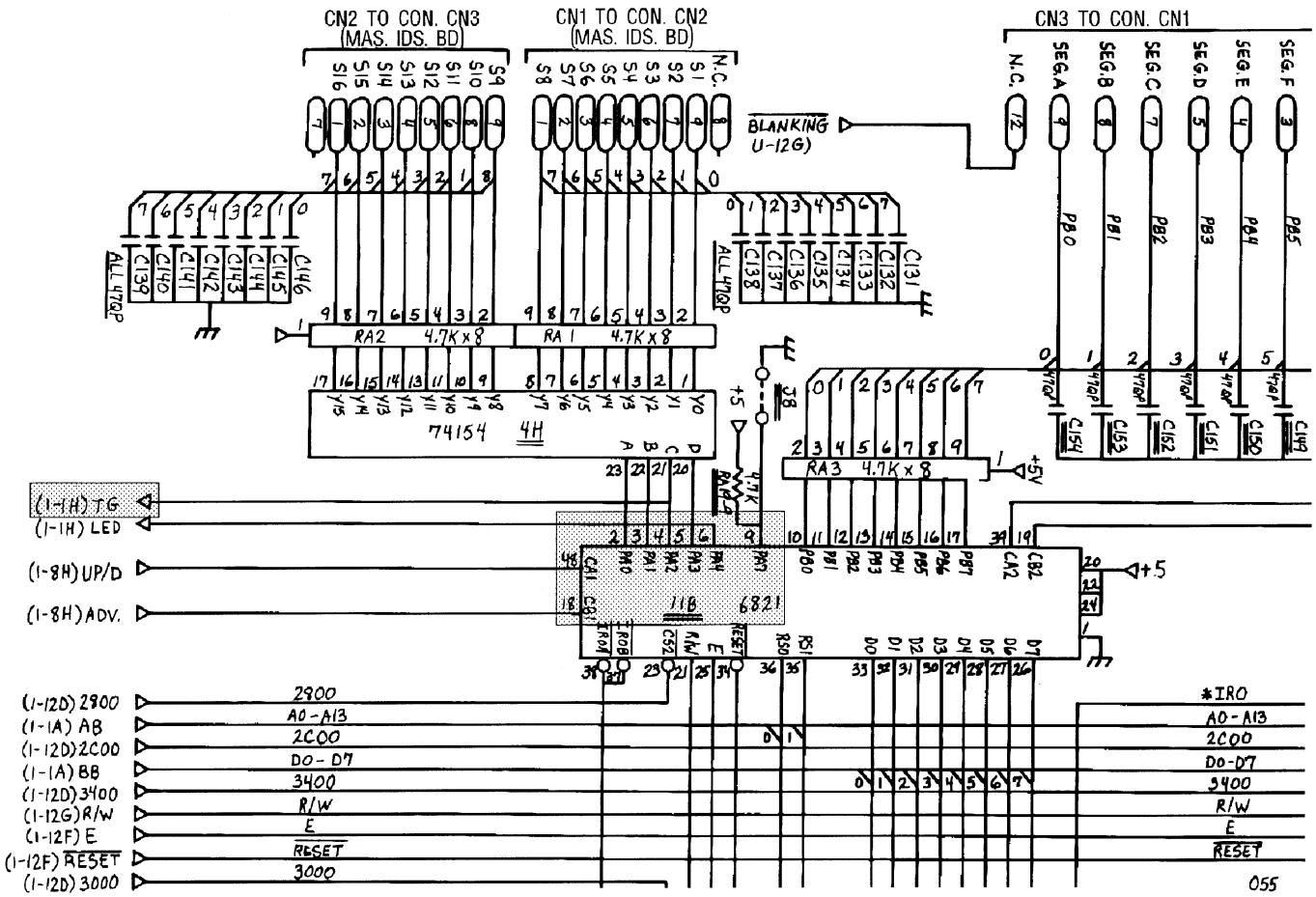
PIA LED	SUSPECT COMPONENT
Stays On:	One of the 6821 PIAs
Flashes 1 Time:	6264 RAM at location D5
Flashes 2 Times:	EPROM at location C5

Fig. 2



PARTIAL SCHEMATIC DEPICTED (From CPU Board Logic Diagram (Sheet 1 of 4)

Fig. 3



PARTIAL SCHEMATIC DEPICTED (From CPU Board Logic Diagram (Sheet 2 of 4)